W-Band High Efficiency InP-Based Power HEMT with 600 GHz $f_{\max}$

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***Abstract*—We have developed 0.1-μm gate-length InAlAs/InGaAs/InP power HEMT's with record efficiency and power gain at 94 GHz. A 200 μm gate-width device has produced 58 mW output power with 6.4 dB power gain and 33% power-added efficiency. The extrapolated $f_{\max}$ of 600 GHz is the highest reported to date for any transistor, and smaller, 30-μm devices fabricated on the same wafer exhibit excellent noise figure (1.4 dB at 94 GHz), demonstrating the applicability of this technology to multifunction MMIC's.**

I. Introduction

W-BAND power transistors are currently of great interest because the implementation of compact monolithic amplifiers incorporating these transistors has the potential for significantly reducing the cost or enhancing the capability of a variety of military and commercial systems. Since transistor amplification at 94 GHz was first demonstrated in 1986 [1], substantial progress has been made improving the millimeter-wave performance of high electron mobility transistors (HEMT's), largely as a result of reduction in gate length and the use of material systems with improved conduction band profiles and transport properties. At 94 GHz, GaAs-based HEMT's with pseudomorphic InGaAs channels, or PHEMT's, have demonstrated single device output powers in the 45–63 mW range with power gains of 3–4 dB [2], [3], and several PHEMT-based W-band power MMIC's have been reported [4]–[7]. However, the output power of these MMIC's has been limited to approximately 100 mW with relatively low associated power-added efficiencies (5–13%), primarily constrained by the performance of the PHEMT devices upon which the amplifiers are based.

In this letter, we report the development of a W-band HEMT, based on the InAlAs/InGaAs/InP material system, with output power comparable to that demonstrated by the GaAs PHEMT's reported previously in [2] and [3], but with significantly higher efficiency and power gain. This InP-based power transistor should enable the development of W-band power MMIC's with enhanced performance for applications in which increased output power or reduced DC power consumption are important.

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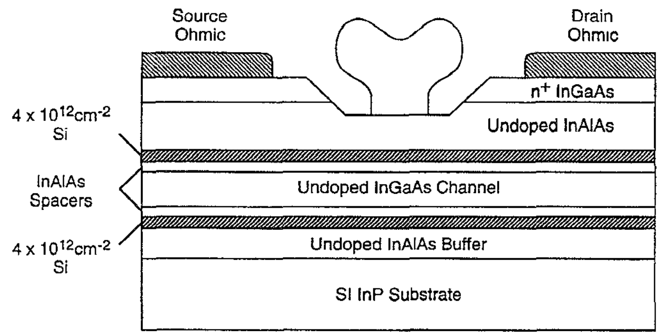


Fig. 1. Cross section of W-band InP-based power HEMT.

II. PHEMT Device Design

The device channel structure, optimized for high gain at 94 GHz, high current handling capability and acceptable breakdown voltage, is shown in Fig. 1. A double heterojunction epitaxial layer structure, in which planar doping is placed both above and below the undoped InGaAs channel, has been employed. The InGaAs channel is pseudomorphic, with 68% indium mole fraction and a thickness of 200 Å. The gate length is 0.1 μm, and the T-shaped gate is composed of TiPtAu. The layer structure was grown by molecular beam epitaxy, and Hall measurements yielded an electron sheet charge density of 3.1×10^{12} cm^{-2} with a mobility of 10 500 cm^2/V · s at 300 K, and 3.1×10^{12} cm^{-2} with a mobility of 28 200 cm^2/V·s at 77 K. The devices were fabricated using a previously reported 0.1 μm T-gate InP-based HEMT process [7] that has demonstrated state-of-the-art W-band low noise device and MMIC performance [8]–[10].

Individual power transistors have a total gate periphery of 200 μm, consisting of four 50-μm-long fingers. These 200 μm InP-based HEMT's were fabricated both as discrete devices and embedded in single-stage MMIC's, as shown in Fig. 2, to facilitate testing at W-band. As seen in the figure, circular via holes created by wet chemistry are placed on each side of the device active region for source grounding and air-bridge interconnects are used to connect to the center source contact. The completed wafers were thinned to 50 μm both to improve thermal properties and to obtain low via inductance for high gain. As depicted in Fig. 1, these devices have not been passivated.

III. Device DC and RF Performance

The 200-μm devices exhibit typical peak dc transconductance g_m of 930 mS/mm, with a maximum value of 980

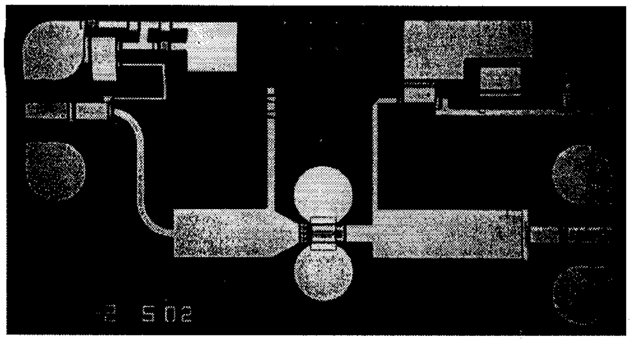


Fig. 2. Single-stage MMIC containing 200 μm gate-width InP power HEMT. Chip size is 1.14 mm × 0.62 mm.

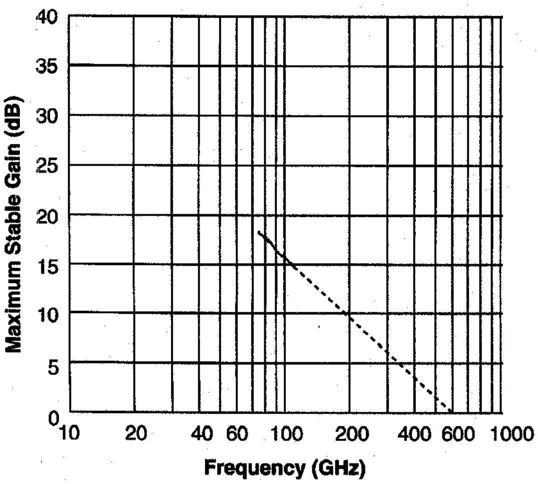
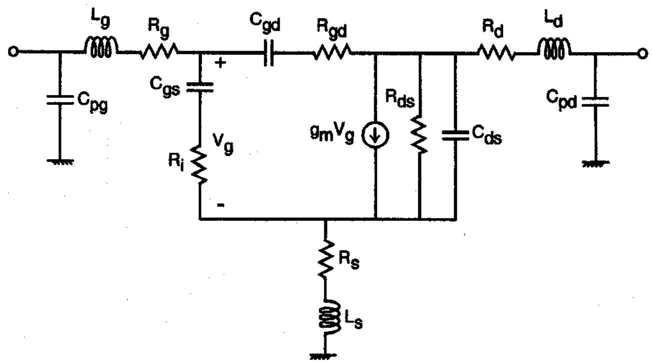


Fig. 3. Maximum stable gain of 0.1 μm × 200 μm InP HEMT, calculated from 75–110 GHz S-parameters measured at V_{ds} = 2 V, I_{ds} = 60 mA. $f_{\max}$ of 600 GHz is obtained by extrapolating at −6 dB per octave.



(a)

Element	Value	Element	Value
g_m	176 mS	R_d	0.12 Ω
C_{gs}	0.242 pF	R_s	0.83 Ω
C_{gd}	0.0048 pF	L_g	12.0 pH
C_{ds}	0.034 pF	L_d	8.0 pH
R_i	1.55 Ω	L_s	1.5 pH
R_{ds}	328 Ω	C_{pg}	0.009 pF
R_{gd}	10.0 Ω	C_{pd}	0.009 pF
R_g	1.6 Ω	τ	0.71 pS

(b)

Fig. 4. Small-signal equivalent circuit model of 0.1 μm × 200 μm InP HEMT at V_{ds} = 2 V, I_{ds} = 60 mA.

mS/mm, at a V_{gs} of 0.1 V. At a drain voltage of 1 V, I_{dss} is typically 50 mA (250 mA/mm) and I_{ds} at a gate voltage of 0.6 V is 115 mA (570 mA/mm). The gate-drain breakdown voltage, defined at 1 mA/mm gate current, is 5.5 V.

Device S-parameters were measured across the 75–110-GHz frequency band using W-band wafer probes, TRL calibration procedures and instrumentation described earlier in [11] and [12]. Maximum stable gain (MSG), derived from S-parameters measured at a drain voltage of 2 V, is plotted in Fig. 3. The MSG is extremely high—16.1 dB at 94 GHz, resulting in an extrapolated maximum frequency of oscillation $f_{\max}$ of 600 GHz. This value of $f_{\max}$ is the highest reported to date for any transistor, including InP-based HEMT's with undoped cap layers [13] and graded InGaAs channels [14].

Maximum current gain cutoff frequency f_t, obtained at a drain bias of approximately 1 V, is 160 GHz. It is worth noting that the design of these devices has been tailored for optimum 94 GHz large-signal operation. Although high f_t is in general believed to be indicative of short electron transit times and therefore high intrinsic device speed, $f_{\max}$ is a more relevant figure of merit for microwave transistors because it denotes the frequency at which power gain, the gain of interest in a high frequency amplifier, has fallen to unity, and includes parasitic effects not accounted for by f_t.

A small-signal equivalent circuit model of the InP HEMT, derived by fitting the W-band S-parameters measured at a V_{ds} of 2 V, is shown in Fig. 4.

Power measurements were performed on-wafer at 94 GHz using the single-stage MMIC shown in Fig. 2. Since the design of this preliminary circuit was based on an inaccurate large signal device model, in practice we found that additional tuning was required at the output to obtain best performance. No input tuning was necessary. The dependence of output power, power-added efficiency (PAE) and gain on input power, measured at a drain bias of 2.8 V, are plotted in Fig. 5. The device generates 58-mW output power with 6.4 dB power gain and 33% PAE. Operated more linearly, output power is 53 mW with 7.5-dB power gain and 30% PAE. Linear gain is 10.0 dB, and a small amount (0.3 dB) of gain expansion is noted at low drive levels, possibly due to heating effects.

Our results are compared with those previously reported for W-band power transistors in Table I. At comparable output power, the InP-based HEMT reported herein exhibits a factor of two improvement in PAE and significantly higher power gain than the PHEMT's reported earlier. Note that the increased power gain will further improve multistage amplifier efficiency by permitting downsizing of driver stage devices. Hence, significant improvement in W-band power MMIC efficiency will be possible by developing circuits based on these InP HEMT's.

TABLE I
COMPARISON OF REPORTED HIGH POWER W-B AND TRANSISTORS

Reference	Transistor Type	Gate Length (μm)	Total Gate Width (μm)	Unit Finger Width (μm)	94 GHz Performance		
					Output Power (mW)	Power Gain (dB)	Power-Added Efficiency (%)
This Work	InP HEMT	0.1	200	50	58	6.4	33
[2]	GaAs PHEMT	0.15	150	75	45	3 0	16
[3]	GaAs PHEMT	0.1	160	20	63	4.0	13

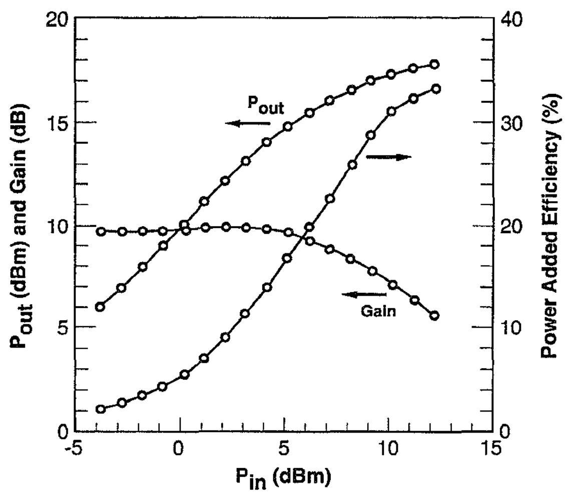


Fig. 5. Measured 94 GHz performance at $V_{ds} = 2.8$ V.

Noise performance of a 30-μm gate width low noise device fabricated on the same wafer was measured at 94 GHz. Minimum noise figure was 1.4 dB with 7.0 dB associated gain. This noise figure is only marginally higher than that of 0.1 μm InP HEMT's optimized specifically for low-noise operation [9], suggesting that high performance power and low noise amplifiers could be integrated together on a common InP MMIC chip.

IV. CONCLUSION

We have reported a 0.1-μm gate-length InP-based power HEMT which has demonstrated significantly improved 94-GHz efficiency and power gain as compared with GaAs-based PHEMT's. In addition, the device exhibits record $f_{\max}$ and excellent noise figure. We believe the superior performance of this device is due primarily to the intrinsic advantages of the InAlAs/InGaAs/InP material system, an optimized layer structure and device design, and the use of a proven high-performance InP HEMT fabrication process.

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